

NASA TM X-1390

PULSE-TRAIN GENERATOR FOR ROCKET CAMERA

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ABSTRACT

The design of a solid-state pulse-train generator to control shutter and film-advance timing for rocket-borne camera experiments is described. The major design objectives were simplicity, flexibility, accuracy, and low power consumption. The timing cycle commences when power is applied, and the circuit recycles continuously until the power is shut off. For experiments in which continuous recycling is not required, the clock can be "clamped"; or binary logic can be added to obtain any number of cycles desired.

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INTRODUCTION

This paper describes a solid-state pulse-train generator to control shutter and film-advance timing in camera experiments on sounding rockets. Circuit simplicity, flexibility, accuracy and low power consumption were the major design objectives. The pulse-train generator produces a time-sequential train of four shutter-timing pulses of different widths, with a fixed interval following each shutter-timing pulse to allow for advancing the film. The timing cycle commences when power is applied, and recycles continuously until the power is shut off. The shutter times are 1/20, 1/10, 1/3, and 1 second, with a fixed 0.6-second spacing following each shutter-timing pulse for film advance. The output of the pulse-train generator activates a solenoid, which in turn operates the camera shutter.

The pulse-train generator was successfully used on NASA Aerobee rocket 4.53 on October 26, 1965, and Aerobee rocket 4.145 on December 2, 1965, both flown from White Sands Missile Range, New Mexico. It is shown mounted on the electronic compartment of the rocket in its unpotted form in Figure 1. Figure 2 is a schematic diagram of the unit.

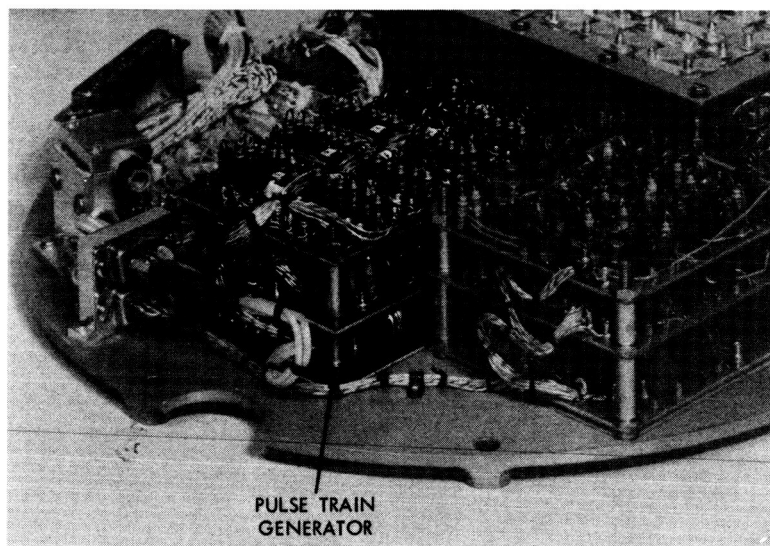


Figure 1—Unpotted unit mounted on electronics compartment base plate.

Figure 2—Schematic diagram of the pulse-train generator.

BLOCK DIAGRAM DESCRIPTION

As depicted in the block diagram (Figure 3), the circuit consists of a unijunction clock driving a 7-stage flip-flop counter. NAND gates are connected to this counter to obtain voltage transition at the desired time to "Set" and "Reset" an output flip-flop. The flip-flop circuit generates the time-sequential pulse train used to control the shutter solenoid.

Since the smallest timing interval is 1/20 second, a clock rate of 20 cps is used (to minimize the number of flip-flop stages required) in the counter. The output pulse widths must be in multiples of the clock rate.

The NPN transistor of the first NAND gate is turned "ON" by the first clock pulse after counter reset (Table 1) and is turned "OFF" by the second clock pulse. The NAND gate output is differentiated and amplified, and the leading edge and trailing edge are used respectively to "Set" and "Reset" the output flip-flop. This results in a 50 millisecond output pulse. The output flip-flop remains at "Reset" until the second NAND gate is turned "ON" by the 14th clock pulse, providing

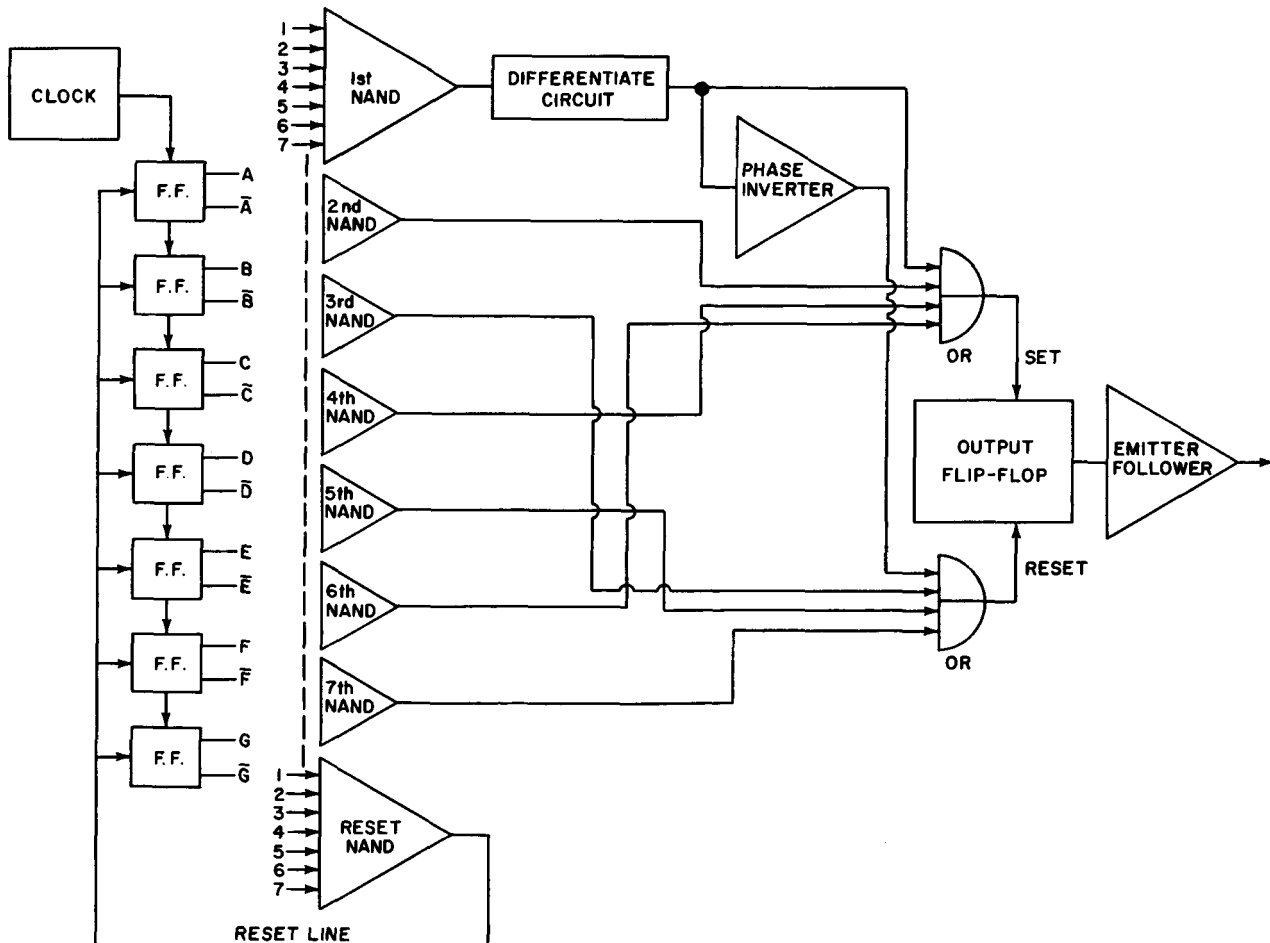


Figure 3—Block diagram of the pulse-train generator.

Table 1

NAND Logic Truth Table.

Flip-Flop	NAND Gate States							
	1st NAND	2nd NAND	3rd NAND	4th NAND	5th NAND	6th NAND	7th NAND	Reset NAND
F.F. 1	1	0	0	0	0	0	1	1
F.F. 2	0	1	0	0	1	1	0	0
F.F. 3	0	1	0	1	0	1	0	1
F.F. 4	0	1	0	1	0	1	0	1
F.F. 5	0	0	1	1	0	0	0	0
F.F. 6	0	0	0	0	1	1	0	0
F.F. 7	0	0	0	0	0	0	1	1
Clock Pulse	#1	#14	#16	#28	#34	#46	#65	#77

an 0.6-second spacing between the first and second output pulse. The leading edge of the second NAND gate is used to "Set" the output flip-flop, and the leading edge of the third NAND gate (16th clock pulse) is used to "Reset" the output flip-flop, resulting in a 100 millisecond output pulse.

NAND gates 4 through 7 are connected to obtain output pulses of 300 and 1,000 milliseconds, with 600 millisecond spacing between pulses. The four "Set" pulses are OR'ed together, as are the four "Reset" pulses, to gate the output flip-flop.

Since the 7-stage flip-flop counter will not run out until the 128th clock pulse, NAND gate number 8 is used to reset the counter on clock pulse No. 77, at which time the pulse-train generator recycles. The recycling continues until power is removed from the timer.

Complementary flip-flops are used to conserve power. In the event that space and weight considerations demand a higher priority than power consumption, micro-logic chips can be substituted for the flip-flops and the NAND gates.

The complete circuit diagram is shown in Figure 2. No detailed circuit description is given since all circuits used are standard logic circuits.

MECHANICAL SPECIFICATIONS

The pulse-train generator is packaged on three single-sided printed circuit boards 4.25 inches long and 2.65 inches wide. The three stacked and potted boards are 2.25 inches high. No attempt was made to miniaturize the final package; estimated conservatively, a thirty percent space saving could have been obtained had time permitted.

The fourteen outputs from the 7-stage flip-flop counters are located on one edge of the top board, and the wiring to the diodes input of each NAND gate is color-coded to facilitate timing changes if necessary.

"Eccofoam" potting is used since the unit is mounted in a pressurized compartment in the rocket where outgassing is not a problem. The potted unit survived 10G sinusoidal and random vibration in all three axes.

ELECTRICAL SPECIFICATIONS

The timer uses two internal power supplies to convert +28VDC rocket battery voltage to +15VDC and +5VDC. These power supplies are pulse-rate modulated for efficiency and regulation. The total power required from the rocket battery is +28V at 6ma. The flight unit tolerates an input voltage change from +25 to +35V, and a temperature change from -20°C to +60°C. The timing accuracy of the output wave form is $\pm 1\%$ within the voltage and temperature limits stated above. The internal power supplies give the pulse-train generator a high degree of noise immunization. Transients as high as 10VDC on the battery line do not affect operation.

CONCLUSIONS

The two rocket flights have demonstrated the reliability of this circuit and its adaptability to rocket work. All of the major design objectives were achieved. The flexibility of the circuit makes it possible to obtain any reasonable pulse width, while the simplicity of the circuit makes duplication easy. With the addition of two flip-flops in the counter string, six output pulses of 1/20, 1/10, 1/3, 1, 3, and 10 seconds with one-second spacing between pulses may be obtained.

For experiments which do not require continuous recycling, the "Reset" NAND gate could be used to activate a clamp to clamp the clock, or binary logic may be added to obtain any desired number of cycles.

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